CLAIMS: I claim:

1. A machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising:
   a. a first sensor having a first sensor output
   b. a threshold detector having a first analog input and a first digital output, said threshold detector comprising:
      i. a first transistor having a first gate
      ii. a second transistor having a second gate
      iii. means for applying said first analog input to said first gate and to said second gate
   c. means for applying said first sensor output as said first analog input.

2. The machine of claim **1** in which:
   a. said first transistor is an n-type MOS transistor
   b. said second transistor is a p-type MOS transistor.

3. The machine of claim **2** in which:
   a. said first transistor has a first transistor drain and a first transistor source
   b. said second transistor has a second transistor drain and a second transistor source
   c. said first transistor drain and said second transistor source are directly connected.

4. The machine of claim **3** in which:
   a. said first transistor source is directly connected to a first power supply rail
   b. said second transistor drain is directly connected to a second power supply rail.

5. The machine of claim **4** in which said first power supply rail has a more negative potential than said second power supply rail.

6. The machine of claim **4** in which said first power supply rail has a more positive potential than said second power supply rail.

7. The machine of claim **1** in which said threshold detector comprises an inverter.

8. The machine of claim **7** in which said inverter comprises said first transistor and said second transistor.

9. The machine of claim **1** in which said threshold detector comprises a digital logic gate.

10. The machine of claim **9** in which said digital logic gate comprises said first transistor and said second transistor.

11. The machine of claim **1** in which said threshold detector is a single-input threshold detector with an implicit threshold level.

12. The machine of claim **1** in which said first transistor and said second transistor are located substantially adjacent to said first sensor, whereby long wires connecting said first sensor, said first transistor, and said second transistor are not required.

13. The machine of claim **1** in which:

a. said first transistor is a minimum-size transistor

b. said second transistor is a minimum-size transistor

whereby the semiconductor chip area occupied by said first transistor and said second transistor is less than would be required for non-minimum-size transistors.

14. A machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising:

a. a multiplicity of threshold detectors, each having:

i. an input line connected to the gates of at least two transistors

ii. a digital output

b. a multiplicity of sensors each having a sensor output provided as input to the input line of one of said multiplicity of threshold detectors

c. means for measuring a multiplicity of elapsed times when said digital outputs of said threshold detectors change states.

15. The machine of claim **13** in which said threshold detectors are single-input threshold detectors with implicit thresholds.

16. The machine of claim **13** in which said threshold detectors are digital logic gates.

17. The machine of claim **13** in which said threshold detectors are inverters.

18. The machine of claim **17** in which said inverters consist of minimum-size transistors.

19. A machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising:

a. a first sensor providing a first sensor output

b. means for initializing said first sensor output to a first sensor output level

c. means for allowing said first sensor output to change in response to incident energy

d. a first digital counter providing a digital elapsed time count

e. means for detecting when said first sensor output reaches a first threshold level, comprising:

i. a first transistor having a first gate

ii. a second transistor having a second gate

iii. a digital indicator output signal for indicating when said first sensor output reaches said first threshold level

iv. means for applying said first sensor output to said first gate

v. means for applying said first sensor output to said second gate

f. means for recording a first value of said digital elapsed time count on the basis of a change in said digital indicator output signal.

20. The machine of claim **19** in which:

a. said means for detecting when said first sensor output reaches said first threshold level is an inverter

b. said digital indicator output signal is the digital output of said inverter.